

Basic Structure of Computers

Week 4 — Arithmetic Micro-operations

Dr. Surekha Lanka

PhD, MTech, MSc, PGDBM, PGDPM, BSc



Four Categories of Micro-operations

Each micro-operation executes in a single clock pulse



Register Transfer

Move binary data
from one register
to another



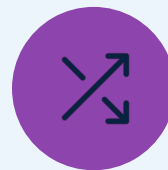
Arithmetic

Add, subtract,
increment, decrement
on numeric data



Logic

Bit manipulation
(AND, OR, XOR)
on non-numeric data



Shift

Shift data left
or right within
a register

Addition & Subtraction

The two fundamental arithmetic micro-operations



Addition

$$R3 \leftarrow R1 + R2$$

Contents of R1 and R2 are added; result stored in R3.



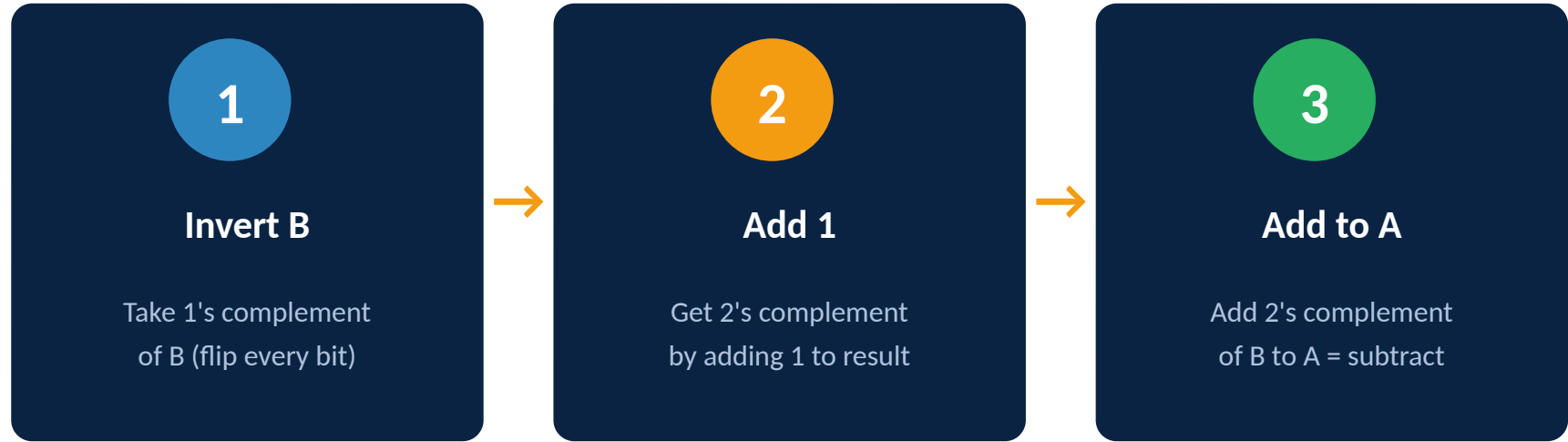
Subtraction

$$R3 \leftarrow R1 + \bar{R2} + 1$$

1's complement of R2 + 1
= 2's complement of R2.
Adding to R1 = subtracting.

How Subtraction Works (A – B)

Subtraction is done through complement-and-add



Addition and subtraction can be combined into one circuit using an XOR gate with each full-adder — the XOR selectively inverts B when subtracting.

Binary Adder — Hardware

Full-Adder

Adds two bits
plus a carry-in

Cascade

Full-adders chained
carry to carry

n-bit

n-bit adder needs
n full-adders

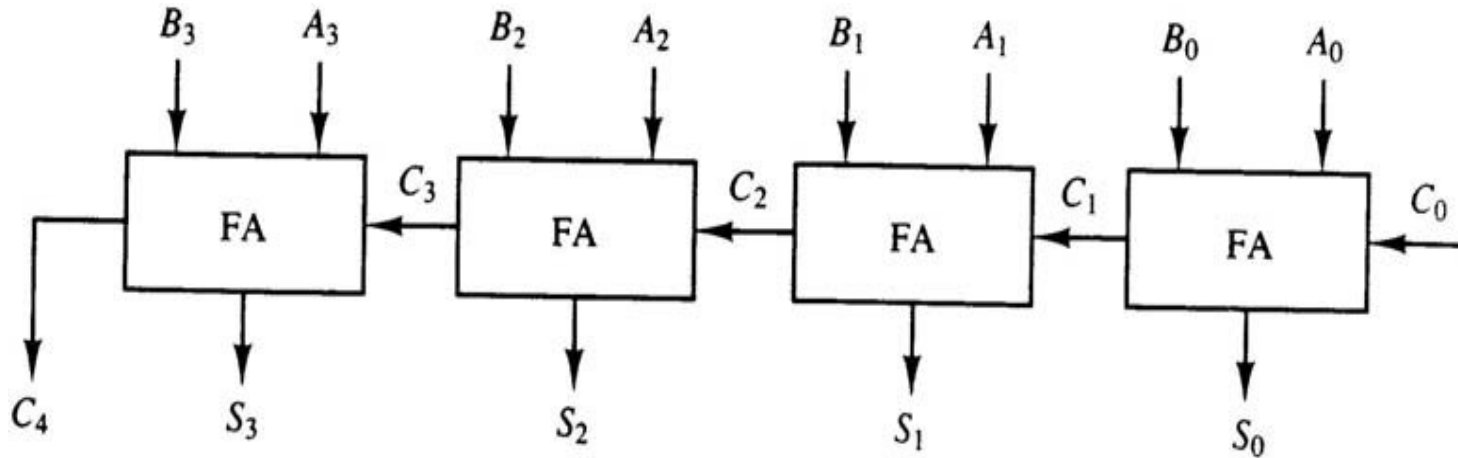


Figure 4-6 4-bit binary adder.

Binary Addition Rules

Addition			Sum	Carry
Addition	Sum	Carry	0	0
0 + 0	0	0		
0 + 1	1	0		
1 + 0	1	0		
1 + 1	0	1		
Addition	Sum	Carry	1	0
0 + 0	0	0		
0 + 1	1	0		
1 + 0	1	0		
1 + 1	0	1		
Addition	Sum	Carry	1	0
0 + 0	0	0		
0 + 1	1	0		
1 + 0	1	0		
1 + 1	0	1		
Addition	Sum	Carry	0	1
0 + 0	0	0		
0 + 1	1	0		
1 + 0	1	0		
1 + 1	0	1		

4-bit Adder-Subtractor Circuit

$M = 0$

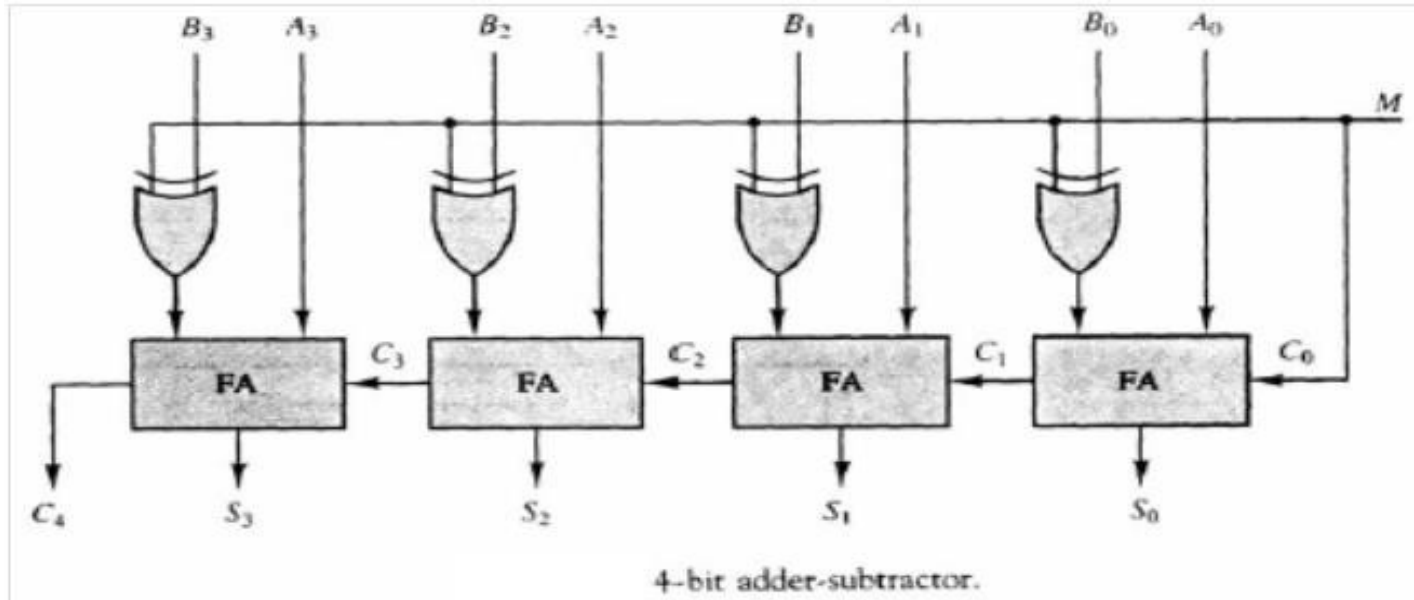
Addition

XOR passes B unchanged

$M = 1$

Subtraction

XOR inverts B (1's comp) + carry-in = 1



What About Multiply & Divide?

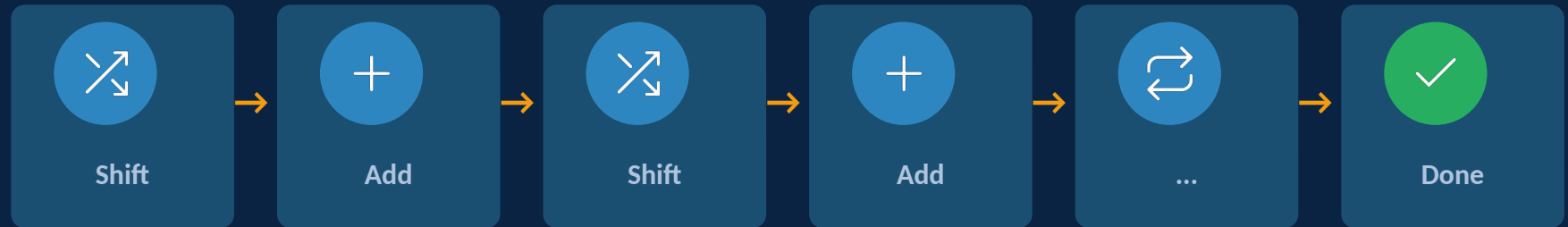
They are NOT single micro-operations



A micro-operation completes in one clock pulse.

Multiply and divide need many clock pulses, so they are implemented as sequences of add-and-shift (or subtract-and-shift).

How Multiply is Built



Week 4 — Summary



Four micro-op types: register transfer, arithmetic, logic, shift



Addition: $R3 \leftarrow R1 + R2$ using cascaded full-adders



Subtraction: complement B then add — uses the same adder hardware



XOR gates + mode bit M combine add/subtract into one circuit



Multiply & divide are multi-cycle — sequences of add & shift

Thank You