

Latches and Flip flops

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Latches and Flip Flops

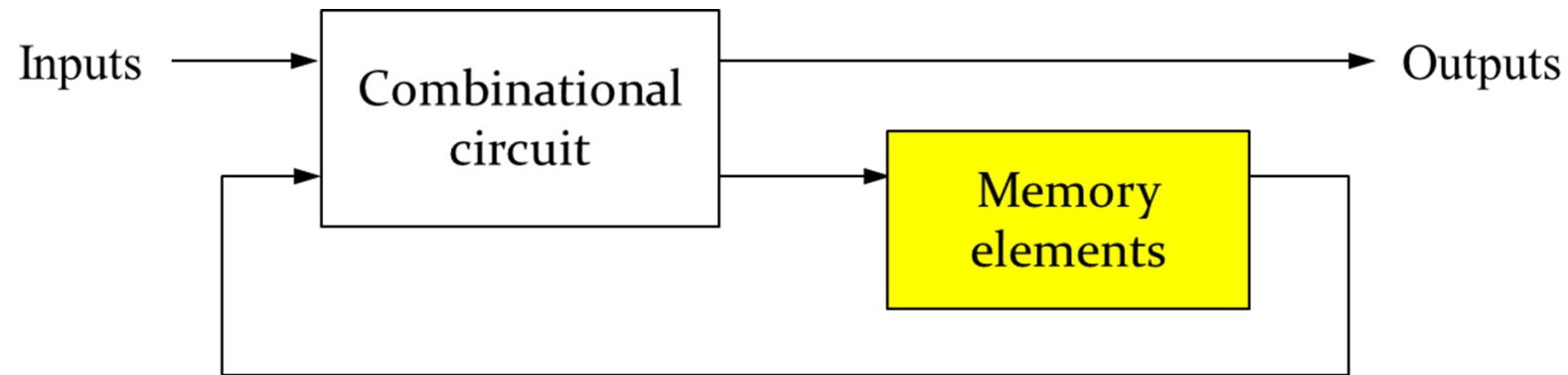
- A latch and a flip-flop are small digital memory circuits that can store one bit of data: either 0 or 1. They are basic building blocks of sequential circuits, registers, and computer memory systems.
- A **latch** is a **level-sensitive** memory device. When its enable signal is active, its output can follow changes in the input when the enable becomes inactive, it keeps the last value.
- Latches are used to design asynchronous sequential circuits.
- Latches have no clock pulse.

Latches and Flip Flops

- A latch and a flip-flop are small digital memory circuits that can store one bit of data: either 0 or 1. They are basic building blocks of sequential circuits, registers, and computer memory systems.
- A flip-flop is an edge-triggered memory device. It reads and stores the input only at a specific instant—usually the rising edge or falling edge of a clock pulse—and then holds that value until the next active clock edge.
- Flip-flops are used to design synchronous sequential circuits.
- Flip-flop has clock pulse.

Sequential Circuits

- The sequential circuit consists of a combinational circuit and storage elements. The previous input/output values are stored in storage elements.



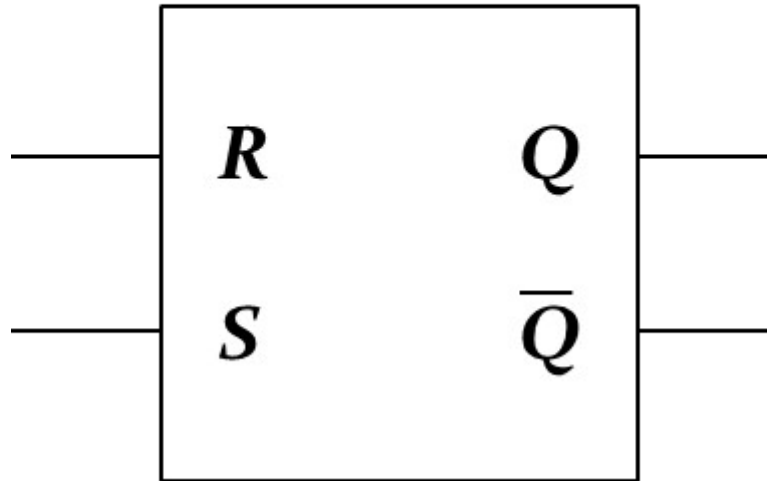
Sequential Circuits

- Here inputs directly are fed into the combinational circuit block.
- The combinational circuit produces outputs with current and prior input values.
- Some states of the combinational circuit are stored in memory elements.
- There are two types of the storage elements:
 - 1) Latch – operated with signal levels, and
 - 2) Flip-Flop – controlled by a clock transition.

SR Latch

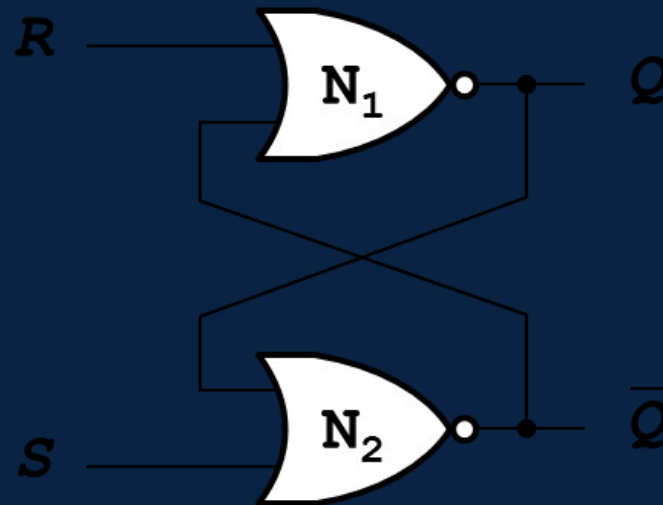
- SR latch is the most fundamental building block using static gates.
- where S and R stand for set and reset.

SR Latch Symbol

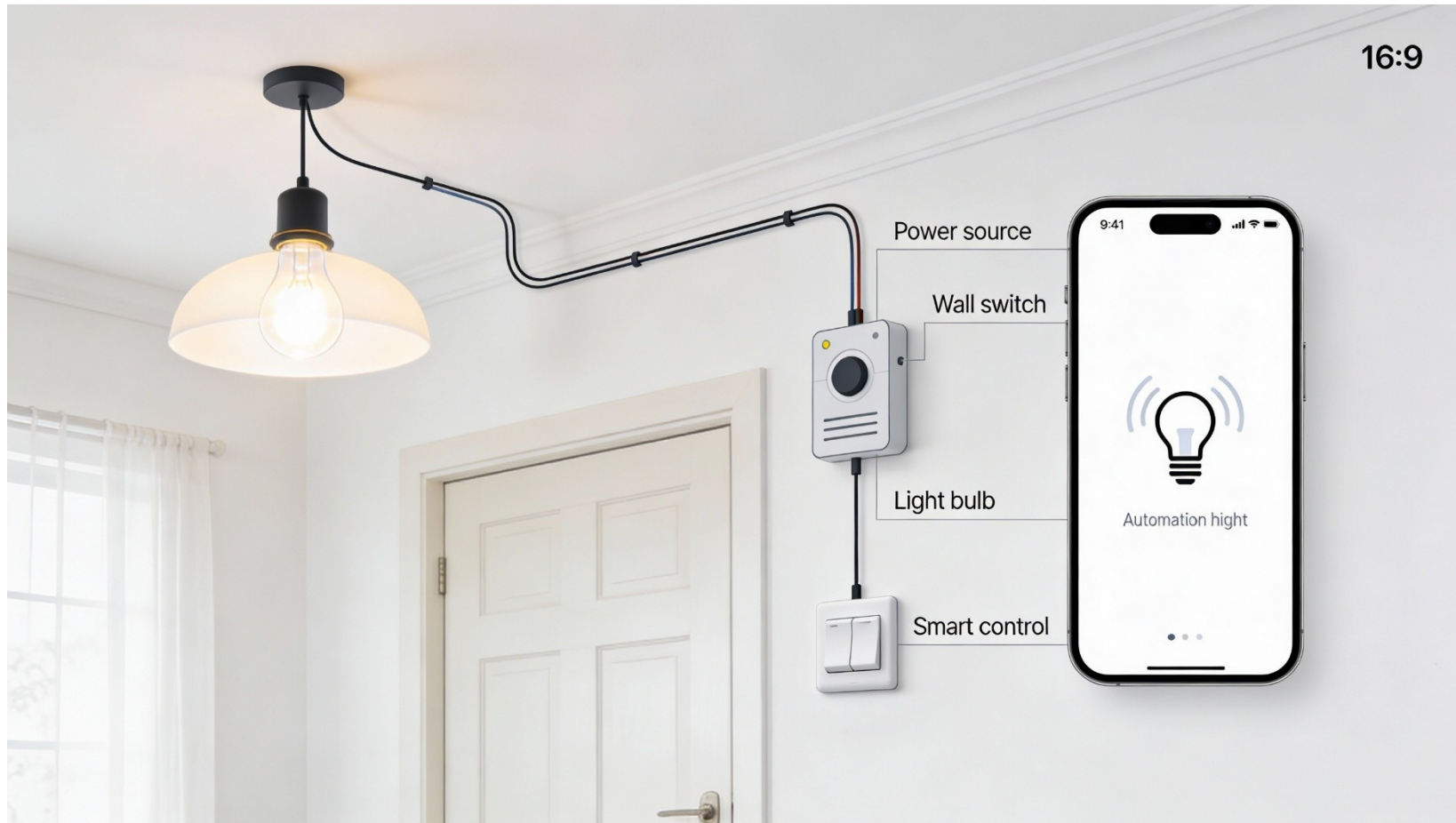


SR Latch

- SR latch is the most fundamental building block using static gates.
- where S and R stand for set and reset.
- SR latch can be designed with two NOR gates/NAND gates.
- The inputs S and R are fed into each NOR gate, and the output of one NOR gate recursively is fed into the input of the other NOR gate



General Real-Life Example: Room Light



Control Imagine a room light system with two push buttons:

SET button (S) → Turns the light ON

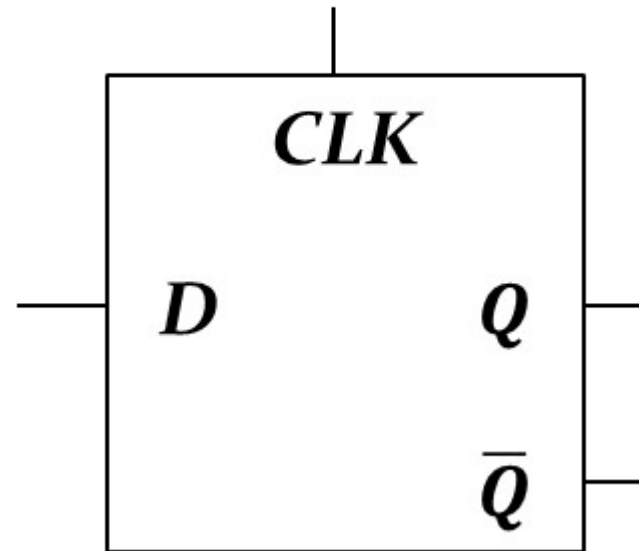
RESET button (R) → Turns the light OFF

Pressing **both buttons together** causes confusion → **Invalid state**
This is exactly how an **SR latch stores memory**.

D Latch

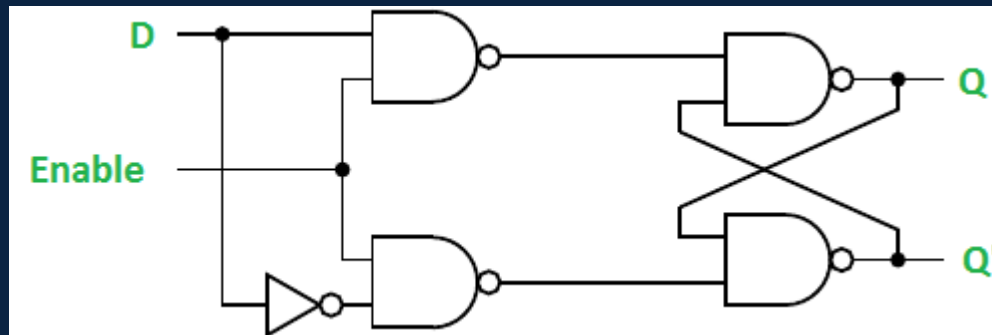
- D latch allows us to avoid this invalid state, where the D latch has two inputs *CLK* and *D*.

D Latch Symbol



D Latch

- SR latch has an invalid state.
- We must do something to avoid the invalid state.
- D latch is similar to SR latch with some modifications made.
- Here, the inputs are complements of each other. The letter in the D latch stands for “data” as this latch stores single bit temporarily.



Note: SR Latch using NAND gates with control , two input connecting NOT gate

General Real-Life Example: Phone Screen Lock



Working:

Press lock button (**E = 1**):

Screen follows your command (ON or OFF)

Release lock button (**E = 0**):

Screen **remains in last state**, even if you touch the screen

This is how a **D latch stores data**.

- Think of a **phone screen lock system**:
- **D (Data)** → Screen state (ON = 1, OFF = 0)
- **Enable (E)** → Lock button pressed
- **Q** → Screen state stored

Flip-Flop

- There are 4 types of Flip flops
- SR Flip-Flop
- D Flip-Flop
- JK Flip-Flop
- T Flip-Flop

SR Flip-Flop

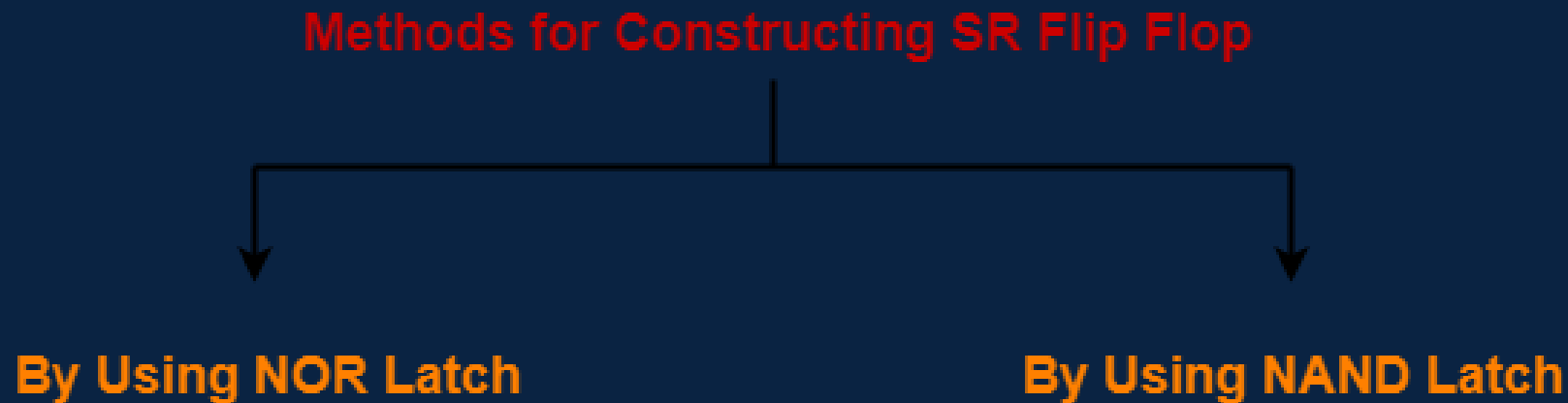
- SR flip flop is the simplest type of flip flops.
- It stands for **Set Reset flip flop**.
- It is a clocked flip flop



Logic Symbol

Construction of SR Flip Flop

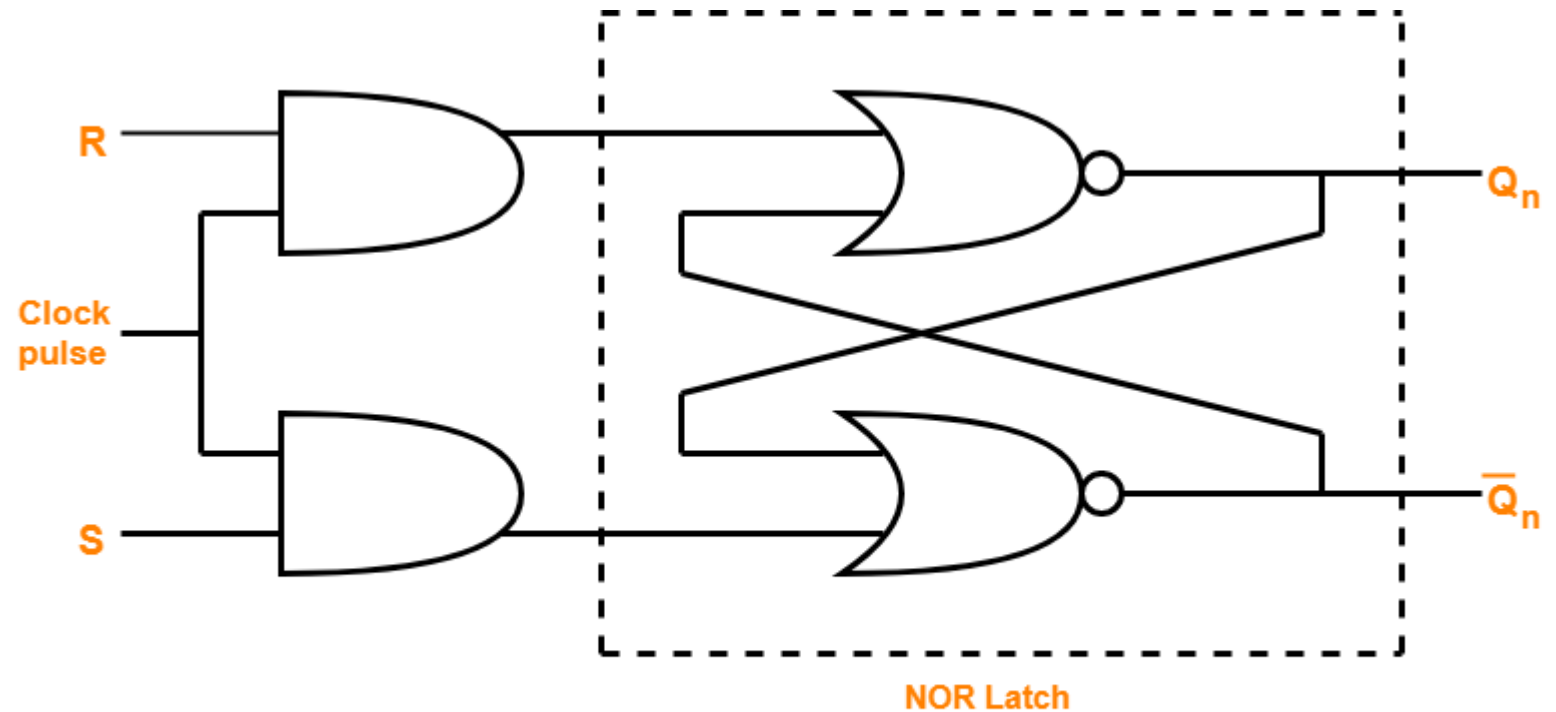
- There are two methods to constructing a SR flip flop



- SR flip-flop operates with only positive clock transitions or negative clock transitions. Whereas, SR latch operates with enable signal.

Construction of SR Flip Flop

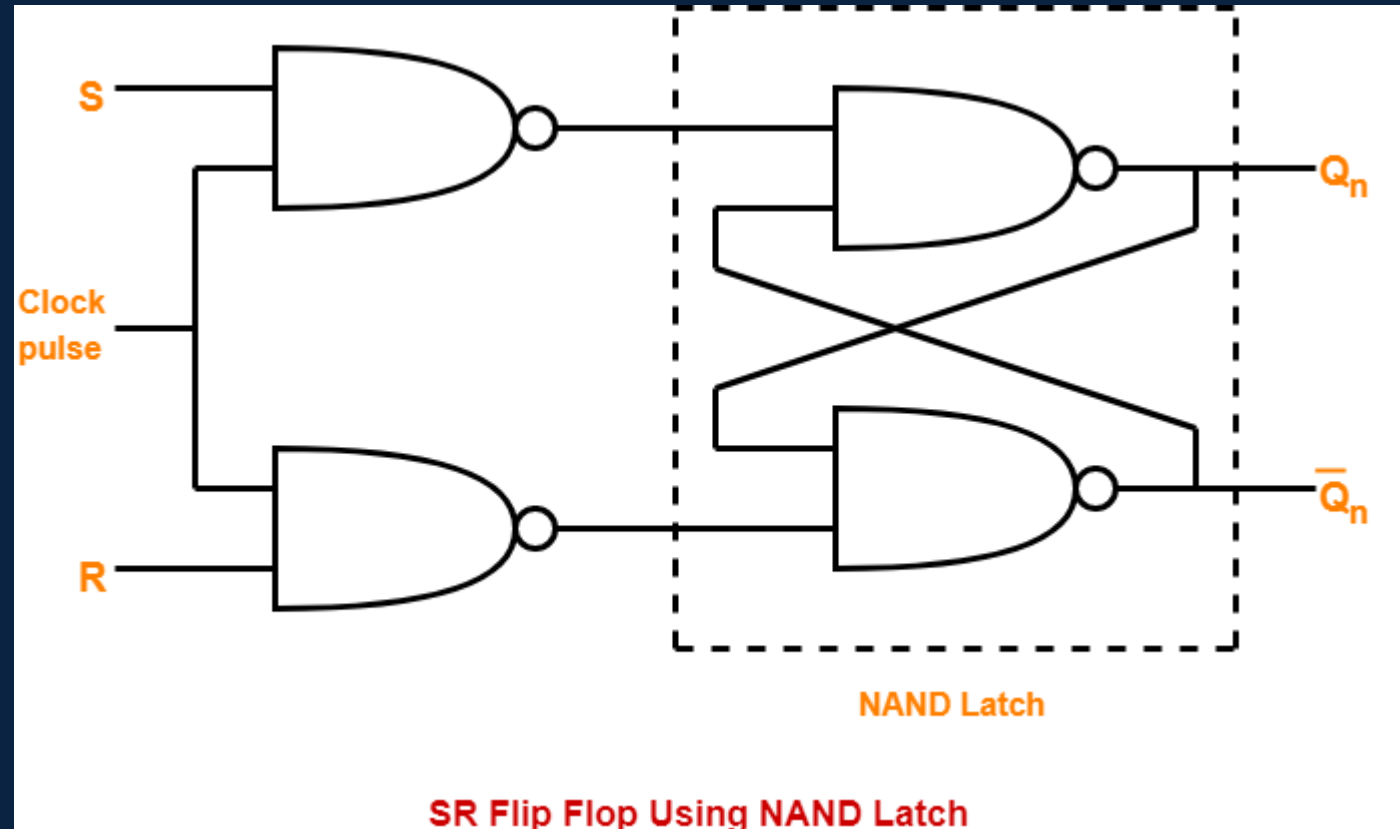
- The logic circuit for SR Flip Flop constructed using NOR latch is as shown below
- NOR latch
- Two NAND gates



SR Flip Flop Using NOR Latch

Construction of SR Flip Flop

- The logic circuit for SR Flip Flop constructed using NAND latch is as shown below
- NAND latch
- Two NAND gates

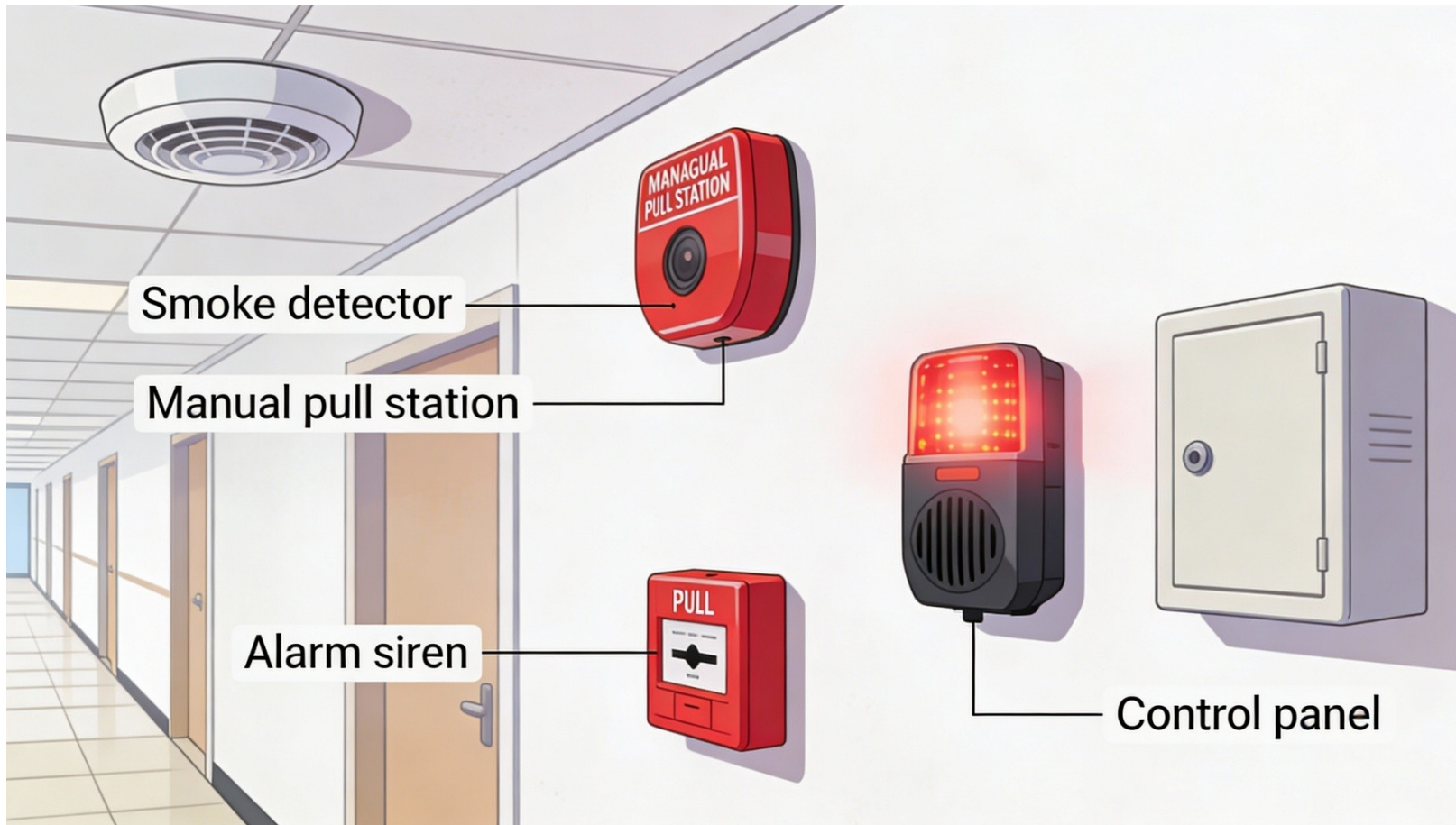


SR Flip Flop

TRUTH TABLE

S	R	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

Real Case Example: Emergency Alarm System (SR Flip-Flop) Scenario



Consider an **emergency alarm system** used in a laboratory or hospital.

Inputs

S (Set) → Emergency detected (fire button pressed)

R (Reset) → Alarm reset by authorized person

Clock → System check pulse

Q (Output) → Alarm status (ON/OFF)

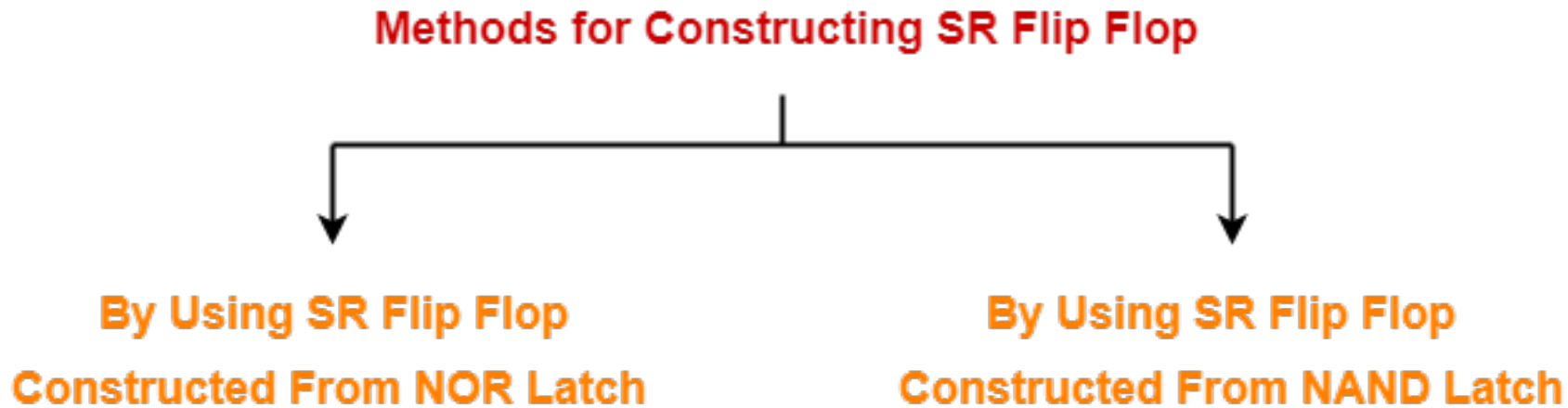
JK Flip-Flop

- JK flip flop is the Jack Kilby.
- The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”.



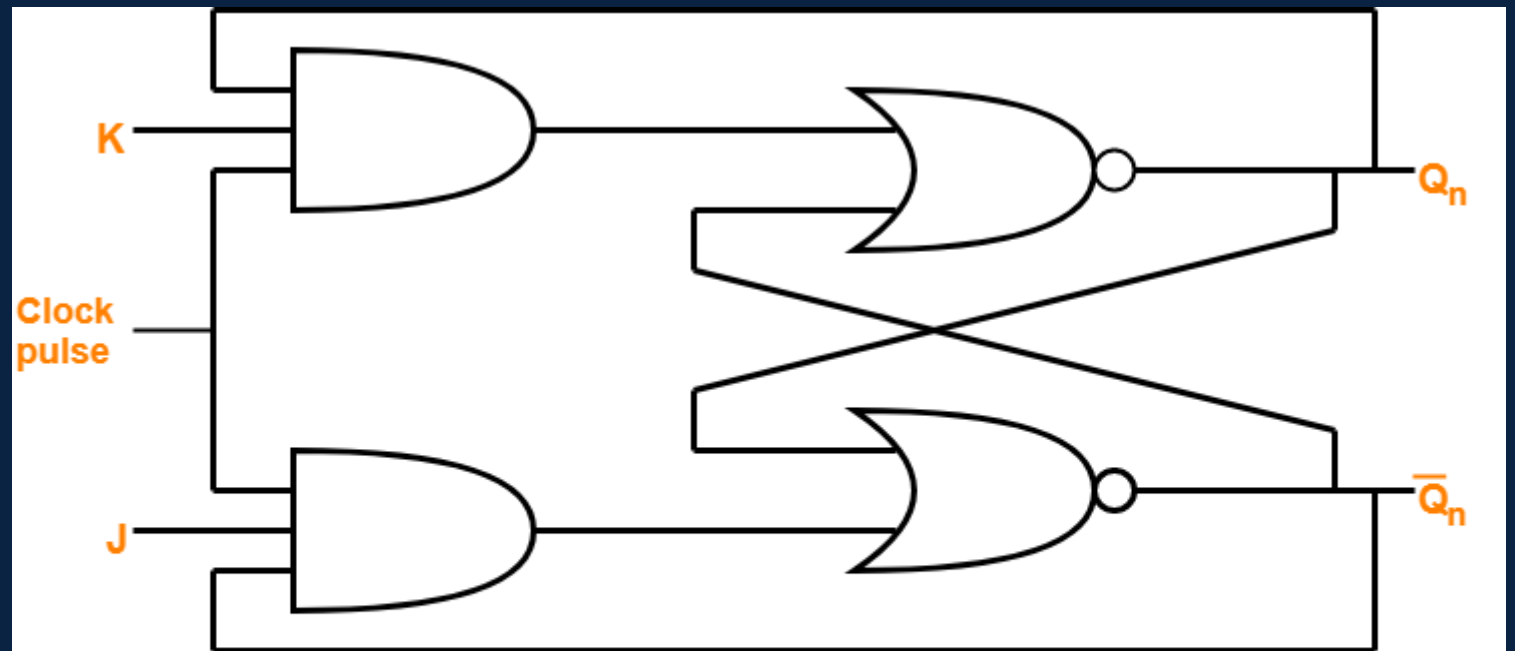
Construction of JK Flip Flop

- There are two methods to constructing a JK flip flop



Construction of JK Flip Flop

- The logic circuit for JK Flip Flop constructed using SR Flip Flop constructed from NOR latch is as shown below-
- SR Flip Flop constructed from NOR latch
- Two other connections



Logic Circuit For JK Flip Flop Using SR Flip Flop

(Constructed From NOR Latch)

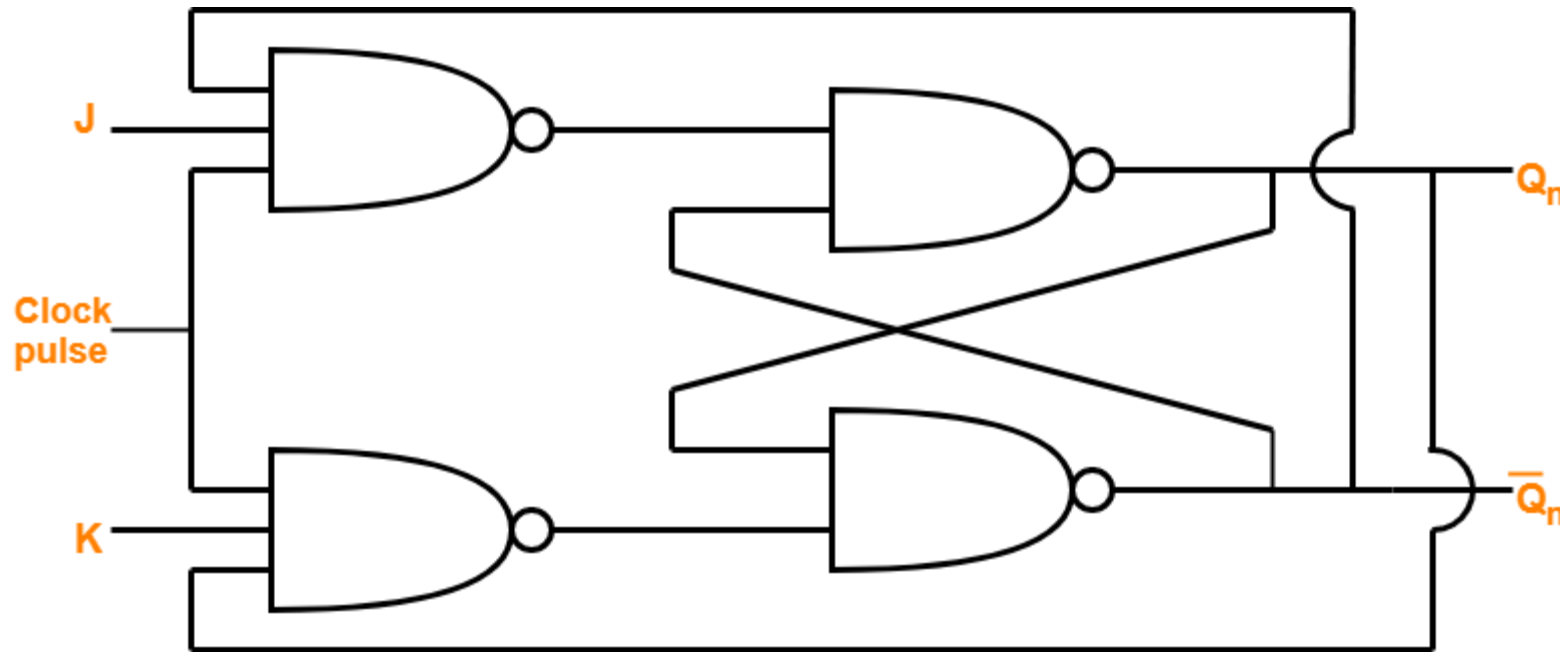
Real Case Example: Office Attendance Control System (JK Flip-Flop) Scenario

- An **office attendance control system** uses a **JK flip-flop** to manage an employee's **IN / OUT** status.
- **Inputs and Output**
- **J (Join / IN)** → Employee enters the office
- **K (Kick-out / OUT)** → Employee leaves the office
- **Clock** → Entry/exit detection pulse
- **Q (Output)** → Attendance status
 - $Q = 1$ → Employee **Inside**
 - $Q = 0$ → Employee **Outside**



Construction of JK Flip Flop

- The logic circuit for JK Flip Flop constructed using SR Flip Flop constructed from NAND latch is as shown below-



Logic Circuit For JK Flip Flop Using SR Flip Flop

(Constructed Using NAND Latch)

Construction of JK Flip Flop

- The JK is similar to SR Flip Flop but there is no change in state when J and K input both low.

TRUTH TABLE

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0